WHAT IS CLAIMED IS:

1. A multiprocessor system having a plurality of processors synchronized after performance of parallel processing, comprising:

a first processor;

a second processor different from said first processor; and

a clock frequency control unit controlling a frequency of a clock being input to said first processor, according to a ratio between a processing time of said first processor and a processing time of said second processor.

2. The multiprocessor system according to claim 1, further comprising a voltage control unit controlling a power supply voltage being supplied to said first processor, according to the frequency of the clock being input to said first processor.

3. The multiprocessor system according to claim 1, further comprising:

a storage unit in which an estimate of the processing time of said first processor and an estimate of the processing time of said second processor are prestored; and

a frequency changing unit changing the frequency of the clock being input to said first processor by controlling said clock frequency control unit according to a ratio between the estimate of the processing time of said first processor and the estimate of the processing time of said second processor that are stored in said storage unit.

4. The multiprocessor system according to claim 1, further comprising:

a storage unit in which a ratio between an estimate of the processing time of said first processor and an estimate of the processing time of said second processor is prestored; and

a frequency changing unit changing the frequency of the clock being input to said first processor by controlling said clock frequency control unit

according to the ratio stored in said storage unit.

5. The multiprocessor system according to claim 1, further comprising a frequency determining unit that causes said clock frequency control unit to lower the frequency of the clock being input to said first processor when processing of said first processor was completed earlier than processing of said second processor in a previous time of processing, and that causes said clock frequency control unit to raise the frequency of the clock being input to said first processor when the processing of said second processor was completed earlier than the processing of said first processor in the previous time of processing.

6. The multiprocessor system according to claim 1, further comprising:

a predicting unit predicting which one of processing of said first processor and processing of said second processor will be completed earlier than the other; and

a frequency changing unit changing the frequency of the clock being input to said first processor by controlling said clock frequency control unit according to the predicted result by said predicting unit.

7. The multiprocessor system according to claim 1, further comprising:

a predicting unit predicting that said first processor will complete processing first when processing of said first processor was completed earlier than processing of said second processor in a previous time of processing, and predicting that said second processor will complete processing first when the processing of said second processor was completed earlier than the processing of said first processor in the previous time of processing; and

a frequency changing unit changing the frequency of the clock being input to said first processor by controlling said clock frequency control unit according to the predicted result by said predicting unit.

8. The multiprocessor system according to claim 1, further comprising:

a predicting unit predicting that said second processor will complete processing first when processing of said first processor was completed earlier than processing of said second processor in a previous time of processing, and predicting that said first processor will complete processing first when the processing of said second processor was completed earlier than the processing of said first processor in the previous time of processing; and

a frequency changing unit changing the frequency of the clock being input to said first processor by controlling said clock frequency control unit according to the predicted result by said predicting unit.

9. The multiprocessor system according to claim 1, further comprising:

a first counting unit counting the processing time of said first processor;

a second counting unit counting the processing time of said second processor; and

a frequency changing unit changing the frequency of the clock being input to said first processor by controlling said clock frequency control unit according to the counted result by said first counting unit and the counted result by said second counting unit.

10. A control method of a multiprocessor system having a plurality of processors synchronized after performance of parallel processing, comprising the steps of:

calculating a ratio between a processing time of a first processor and a processing time of a second processor; and

controlling a frequency of a clock being input to said first processor according to said calculated ratio.

11. The control method of the multiprocessor system according to claim 10, further comprising the step of controlling a power supply voltage

being supplied to said first processor according to the frequency of the clock being input to said first processor.

12. The control method of the multiprocessor system according to claim 10, wherein said step of controlling the frequency of the clock being input to said first processor includes the steps of

calculating a ratio between a prestored estimate of the processing time of said first processor and a prestored estimate of the processing time of said second processor, and

changing the frequency of the clock being input to said first processor according to the calculated ratio.

13. The control method of the multiprocessor system according to claim 10, wherein said step of controlling the frequency of the clock being input to said first processor includes the step of changing the frequency of the clock being input to said first processor according to a prestored ratio of an estimate of the processing time of said first processor and an estimate of the processing time of said second processor.

14. The control method of the multiprocessor system according to claim 10, wherein said step of controlling the frequency of the clock being input to said first processor includes the step of lowering the frequency of the clock being input to said first processor in the case where processing of said first processor was completed earlier than processing of said second processor in a previous time of processing, and raising the frequency of the clock being input to said first processor in the case where the processing of said second processor was completed earlier than the processing of said first processor in the previous time of processing.

15. The control method of the multiprocessor system according to claim 10, wherein said step of controlling the frequency of the clock being input to said first processor includes the steps of

predicting which one of processing of said first processor and

processing of said second processor will be completed earlier than the other, and

changing the frequency of the clock being input to said first processor according to the predicted result.

16. The control method of the multiprocessor system according to claim 15, wherein said step of predicting which one of the processing of said first processor and the processing of said second processor will be completed earlier than the other includes the step of predicting that the processing of said first processor will be completed first in the case where processing of said first processor was completed earlier than processing of said second processor in a previous time of processing, and predicting that the processing of said second processor will be completed first in the case where the processing of said second processor was completed earlier than the processing of said first processor in the previous time of processing.

17. The control method of the multiprocessor system according to claim 15, wherein said step of predicting which one of the processing of said first processor and the processing of said second processor will be completed earlier than the other includes the step of predicting that the processing of said second processor will be completed first in the case where processing of said first processor was completed earlier than processing of said second processor in a previous time of processing, and predicting that the processing of said first processor will be completed first in the case where the processing of said second processor was completed earlier than the processing of said first processor in the previous time of processing.

18. The control method of the multiprocessor system according to claim 10, wherein said step of controlling the frequency of the clock being input to said first processor includes the steps of

counting the processing time of said first processor,

counting the processing time of said second processor, and

changing the frequency of the clock being input to said first

processor according to the counted processing time of said first processor and the counted processing time of said second processor.